Claims

[c1] 1. A three-dimensional memory structure, comprising:

a first stack circuit, having:

a pair of first conductive layers;

a first first-type polysilicon layer between the first conductive layers;

a first second-type polysilicon layer between the first first-type polysilicon layer and one of the first conductive layers; and

a first anti-fuse between the first first-type polysilicon layer and the other one of the first conductive layers; and

a second stack circuit crossing over the first stacked circuit, having:

a pair of second conductive layers;

a second second-type polysilicon layer between the second conductive layers;

a second first-type polysilicon layer between the second second-type polysilicon layer and one of the second conductive layers; and

a second anti-fuse between the second second-type polysilicon layer and the other one of the second conductive layers.

[c2] 2. The memory structure of claim 1, wherein the first first-type polysilicon layer and the second first-type polysilicon layer include an n-type polysilicon layer.

[c3] 3. The memory structure of claim 2, wherein the first second-type polysilicon layer and the second second-type polysilicon layer include a p-type polysilicon layer.

[c4] 4. The memory structure of claim 1, wherein the first first-type polysilicon layer and the second first-type polysilicon layer include a p-type polysilicon layer.

[c5] 5. The memory structure of claim 4, wherein the first second-type polysilicon layer and the second second-type polysilicon layer include an n-type polysilicon layer.

[c6] 6. The memory structure of claim 1, wherein the first anti-fuse and the second anti-fuse include an oxide layer.

[c7] 7. The memory structure of claim 1, wherein the first conductive layers and the second conductive layers include a tungsten silicide layer.

[c8] 8. The memory structure of claim 1, wherein the first conductive layers and the second conductive layers include a titanium nitride layer.

[c9] 9. A three-dimensional memory structure, comprising:
a C/A/N/P/C line, wherein N is an n-type polysilicon layer, C is a conductive layer, A is an anti-fuse and P is a p-type polysilicon layer; and
a C/A/P/N/C line crossing over the C/A/N/P/C line.

[c10] 10. The memory structure of claim 9, wherein the anti-fuse structure includes an oxide layer.

[c11] 11. The memory structure of claim 9, wherein the conductive layer includes a tungsten silicide layer.

[c12] 12. The memory structure of claim 9, wherein the conductive layer includes a titanium silicide layer.

[c13] 13. A method of forming a three-dimensional memory structure, comprising the steps of:

providing a substrate;

forming an N/C/A/N stack structure over the substrate, wherein N is an n-type polysilicon layer, C is a conductive layer and A is an anti-fuse; and

forming a P/C/A/P stack structure over the substrate such that the P/C/A/P stack structure crosses over the N/C/A/N stack structure, wherein P is a p-type polysilicon layer.

[c14] 14. The method of claim 13, wherein the step of forming the N/C/A/N stack structure over the substrate includes the sub-steps of:

forming a first n-type polysilicon layer over the substrate;

forming a first conductive layer over the first n-type polysilicon layer;

forming a first anti-fuse over the first conductive layer;

forming a second n-type polysilicon layer over the first anti-

fuse; and

patterning the second n-type polysilicon layer, the first anti-fuse, the first conductive layer and the first n-type polysilicon layer to form the N/C/A/N stack structure.

[c15] 15. The method of claim 14, wherein the first conductive layer is fabricated using a material selected from a group consisting of tungsten silicide and titanium silicide.

[c16] 16. The method of claim 13, wherein the step of forming a P/C/A/P stack structure over the substrate includes the sub-steps of:

forming a first p-type polysilicon layer over the N/C/A/N stack structure;

forming a second conductive layer over the first p-type polysilicon layer;

forming the second anti-fuse over the second conductive layer;

forming a second p-type polysilicon layer over the second anti-fuse; and

patterning the second p-type polysilicon layer, the second anti-fuse, the second conductive layer and the first p-type polysilicon layer to form the P/C/A/P stack structure.

[c17] 17. The method of claim 16, wherein step of patterning the second p-type polysilicon layer, the second anti-fuse, the second conductive layer and the first p-type polysilicon layer

includes using the first anti-fuse as an etching stop layer.

[c18] 18. The method of claim 16, wherein the second conductive layer is fabricated using a material selected from a group consisting of tungsten silicide and titanium silicide.

[c19] 19. The method of claim 13, wherein the first anti-fuse and the second anti-fuse include an oxide layer.

[c20] 20. A method of forming a three-dimensional memory structure over a substrate, comprising the steps of:
forming a first stack layer over the substrate, wherein the first stack layer includes, from the substrate upwards, a first n-type polysilicon layer, a first conductive layer, a first anti-fuse and a second n-type polysilicon layer;
patterning the first stack layer to form a first stack circuit;
forming a second stack layer over the first stack circuit, wherein the second stack layer includes, from the first stack circuit upwards, a first p-type polysilicon layer, a second conductive layer, a second anti-fuse and a second p-type polysilicon layer; and
patterning the second stack layer to form a second stack circuit, wherein the second stack circuit crosses over the first stack circuit.

[c21] 21. The method of claim 20, wherein the step of patterning the second stack layer includes using the first anti-fuse as an

etching stop layer.

[c22] 22. The method of claim 20, wherein the first anti-fuse and the second anti-fuse include an oxide layer.

[c23] 23. The method of claim 20, wherein the first conductive layer and the second conductive layer include a tungsten silicide layer.

[c24] 24. The method of claim 20, wherein the first conductive layer and the second conductive layer include a titanium silicide layer.